The Design of 5 GHz Voltage Controlled Ring Oscillator Using Source Capacitively Coupled Current Amplifier

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Abstract **— A 5 GHz voltage controlled ring-oscillator (VCO) has been designed using 0.18 μm CMOS technology. Source Capacitively Coupled Current Amplifier (SC3A) is adopted to realize this VCO. Because of the band-pass characteristic of the SC3A, this VCO exhibits the low noise performance with a large tuning range. It can operate from 4.3 GHz up to 6.1 GHz with a phase noise of about -85 dBc/Hz at 1 MHz frequency offset. For the 2 V supply voltage, the power consumption is about 80 mW.**

I. INTRODUCTION

VCOs are widely used in wireless and optical communication systems . In the wireless transmission systems, the VCO is used for the frequency synthesizer to generate the local oscillating signal for the modulation and demodulation of the RF signal. In digital optical transmission systems, VCOs are used as the core circuit of the clock recovery circuit, whose output signal is used for data decision and regeneration.

Wireless and optical communication systems have shown a explosive growth during the last few years. This exponential growth has driven the need for more compact, more cost-effective, fully integrated, low noise, low power voltage-controlled oscillator (VCO).

As the feature size getting smaller, CMOS technologies became attractive for the realization of high speed and high frequency ICs. Nowadays, down to 0.13 μm CMOS process is available for circuit fabrication. In this work, we report a 5 GHz voltage controlled ring oscillator, which is fabricated in a 0.18 μm CMOS technology. This VCO is suitable for half rate 10 GHz clock recovery circuit of 10 Gb/s SDH optical receiver and the frequency synthesizer of 5 GHz Wireless LAN [1]- [3].

II.VCO DESIGN

In order to get high stability, low phase noise and low cross-talk, to increase the quality factor Q of the resonant loop is quite important for the VCO design. To realize the high Q factor of this resonant loop, there are many circuit topologies which can be chosen.

Because of the band-pass nature of the resonant tank, the LC oscillator topology can provide the lowest phase noise for a given amount of power. But the passive element of the resonant loop, the high Q factor, high resonate frequency inductor is hard to be monolithically integrated using actual CMOS technology, also the on-chip inductor occupies a very large chip area. A ring-oscillator topology is adopted for VCO design, because of its large tuning range, small chip area, and its easy integration.

Both single-ended and differential amplifier can be used to realize the ring oscillator. But the differential amplifier has some advantages as given below:

1) High common mode rejection characteristics which decrease the sensitivity of the ring oscillator to the common mode noise and the power supply and substrate distortion.
2) Even stages of the differential amplifiers also can realize the negative feedback and generate the suitable phase delay for the oscillation.
3) Differential amplifier can operate at higher speed or frequency than single-ended amplifier.

The simple differential amplifier, shows a transfer function like a low-pass filter. It is sensitive to the low frequency noise. Here, a differential source capacitively coupled current amplifier is used as the basic stage of VCOs. Fig 1. shows the schematic of the differential source capacitively coupled current amplifier:

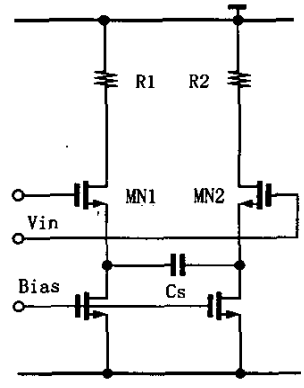

Fig. 1. Schematic of the differential SC3A

A coupled capacitor C_s is inserted at the source of the differential amplifier, the circuit performance of restraining noise can be significantly improved.

For small signal analysis of SC3A, the single-ended source capacitively coupled current amplifier(SSC3A) as shown in Fig 2(a) is analyzed. The Fig. 2(b) is the equivalent circuit of SSC3A.

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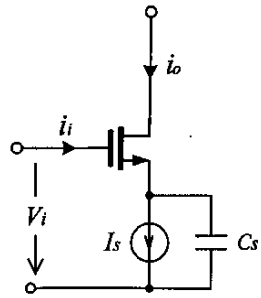
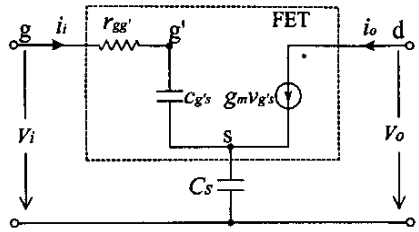


(a) SSC3A



(b) equivalent circuit of SSC3A

Fig. 2 SSC3A circuit and its equivalent circuit

From the equivalent circuit, the real part of the input impedance of SSC3A is :

$$r_{i\_C^3A} = r_{gg'} - \frac{g_m}{(2\pi f)^2 C_{g's} C_s} \tag{1}$$

The real part of the input conductance of SSC3A is :

$$g_{i\_C^3A} = \frac{1}{r_{gg'}} \cdot \frac{f^2 - \frac{g_m}{(2\pi)^2 C_{g's} C_s r_{gg'}}}{\left[f - \frac{g_m}{(2\pi)^2 C_{g's} C_s r_{gg'} f}\right]^2 + \left[\frac{C_{g's} + C_s}{2\pi C_{g's} C_s r_{gg'}}\right]^2} \tag{2}$$

From the equation (2), we can get, when

$$f < f_0 = \frac{1}{2\pi}\sqrt{\frac{g_m}{C_{g's} C_s r_{gg'}}}$$

and $$C_s < C_{s0} = \frac{g_m}{(2\pi f_0)^2 C_{g's} r_{gg'}} \tag{3}$$

the $r_{i\_C^3A}$ and $g_{i\_C^3A}$ will be a negative value.

For the amplitude of the transconductance of SSC3A, it can be derived from the equivalent circuit,

$$|G_m| = \frac{\frac{g_m}{2\pi C_{g's}}}{r_{gg'}\sqrt{\left[f - \frac{g_m}{(2\pi)^2 C_{g's} C_s r_{gg'} f}\right]^2 + \left[\frac{C_{g's} + C_s}{2\pi C_{g's} C_s r_{gg'}}\right]^2}} \tag{4}$$

we can get :

1) when $f \to 0$ and $f \to \infty$, $|G_m| \to 0$

2) when $f = f_{Gm} = \sqrt{\frac{g_m}{(2\pi)^2 C_{g's} C_s r_{gg'}}}$, $|G_m| = |G_m|_{\max}$, then the amplitude of the transconductance shows the band-pass characteristic. The center frequency is f_{Gm}.

According to the theoretical analysis, by tuning the capacitance of the coupled capacitor C_s, the input transconductance becomes a negative value and the frequency response shows a band-pass characteristic, which will increase the Q factor of the oscillator and the capability to restrain noise and crosstalk.

Based on the analytic result, the system block of the SC3A ring oscillator is shown in Fig. 3.

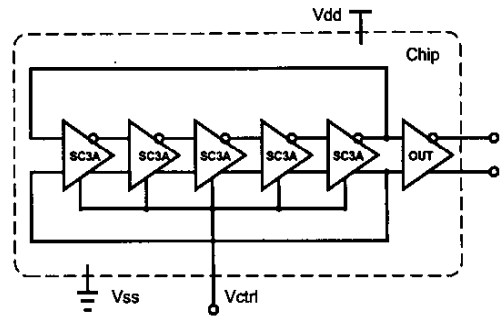


Fig. 3. System block of the SC3A ring oscillator

This ring oscillator consists of five stages of differential SC3A with a negative feedback and the output buffer which provide a 50 Ω output impedance matching to the system environment.

The schematic of the single stage differential SC3A is shown in Fig 4.

MN1,2, MGCS1,2, R1,2, Css are used for the source capacitively coupled current amplifier. MSF1,2 and MDF1,2 build up differential source followers for level-shifting and impedance transforming.

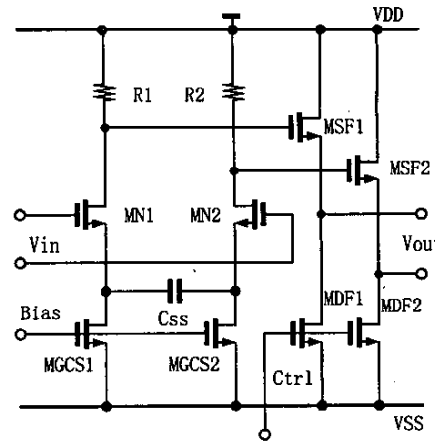


Fig . 4. The schematic of the differential SC3A

AC simulation is used to get the frequency response of a single stage differential SC3A , in Fig. 5 it shows a band-pass characteristic with the center frequency of about 5 GHz. Compared to the low-pass characteristic of the differential amplifier, the differential SC3A shows a good performance in low frequency noise restraining because of its band-pass characteristic.

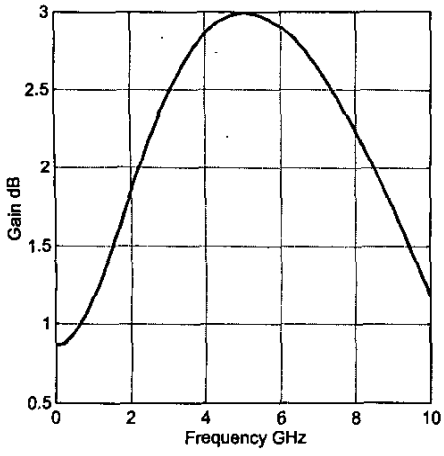


Fig. 5 . The frequency response of a single stage SC3A ampifier

III. Manufacturing Aspects

This ring oscillator was fabricated using a 0.18 μm single poly, six-metal, triple well CMOS technology by means of the CMP program, France. The transit frequency f_T of this very deep sub-micron CMOS technology is about 40 GHz. The microphotograph of the ring oscillator IC is shown in Fig 6.

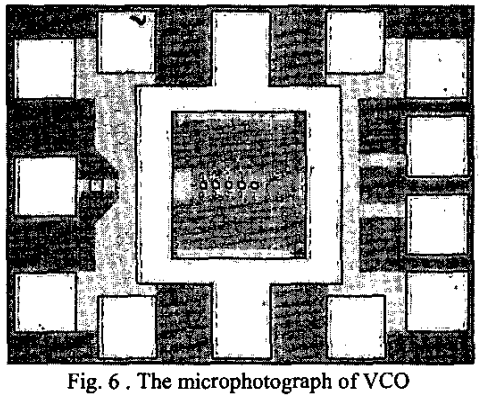


Fig. 6 . The microphotograph of VCO

The chip area is 0.46 x 0.6 mm^2. Layout was carried out preserving the symmetry of the differential amplifier to reduce offset from layout and processing. All of the devices, power planes and ground planes are arranged to prevent interference of signals. To lighten the burden of inspection, pads are allocated with compatibility to the microwave on-wafer probing system.

IV. Experiment Results

The DC current at 2 V supply voltage is about 40 mA, corresponding to a power consumption of 80 mW.

The ring oscillator was measured on-wafer using a CASCADE probe station and the Anritsu spectrum analyzer. The single –ended output spectrum of the ring oscillator is shown in Fig. 7. Single-ended output power is –15 dBm at a 50 Ω load at 4.9 GHz.

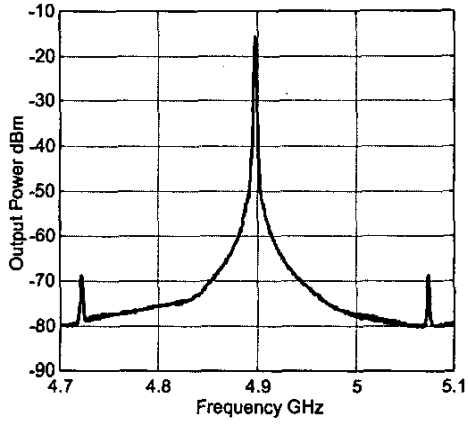


Fig. 7. The single-ended output spectrum of SC3A VCO

From Fig. 8, it can be seen that the frequency of the SC3A VCO can be tuned linearly from 4.3 GHz up to almost 6.1 GHz. The deviation between the simulation result and the measurement result is smaller than 3 %.

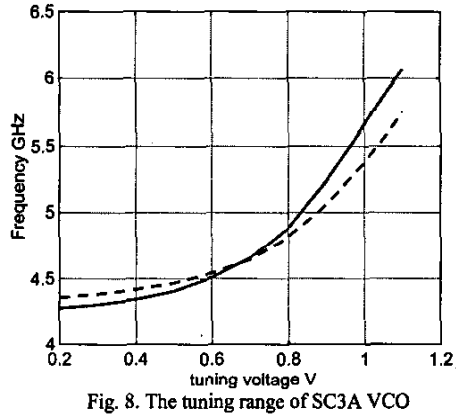


Fig. 8. The tuning range of SC3A VCO (dashed line is the simulation result, solid line is the measurement result)

The phase noise, measured by an Anritsu spectrum analyzer, is -85 dBc/Hz at 1 MHz offset from the 5 GHz signal. At 10 MHz offset, the phase noise is -105dBc/Hz for the same 5 GHz signal.

V. Conclusion

A 5 GHz voltage controlled ring oscillator using differential source capacitively coupled current amplifier was designed and fabricated using a 0.18 μm single-poly, six-metal, tripple-well CMOS technology. This design yields -85 dBc/Hz phase noise at an offset frequency of 1 MHz and -105 dBc/Hz phase noise at an offset frequency of 10 MHz. This VCO shows a wide linear tuning range from 4.3 GHz up to 6.1 GHz. The power consumption is 80 mW at a 2 V supply voltage.

Reference

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[2] Hamid Rategh, Hirad Samavati, and Thomas H. Lee " A CMOS Frequency Synthesizer with an Injection-Locked Frequency Divider for a 5 GHz Wireless LAN Receiver" IEEE Journal of Solid-State Circuits, VOL. 35, NO.5, May 2000, pp. 780-787

[3] Hamid Rategh, Hirad Samavati, and Thomas H. Lee " A CMOS Frequency Synthesizer with an Injection-Locked Frequency Divider for a 5 GHz Wireless LAN Receiver" IEEE Journal of Solid-State Circuits, VOL. 35, NO.5, May 2000, pp. 780-787